ABSTRACT

A reconfigurable digital processing system for space includes the utilization of field programmable gate arrays utilizing a hardware centric approach to reconfigure software processors in a space vehicle through the reprogramming of multiple FPGAs such that one obtains a power/performance characteristic for signal processing tasks that cannot be achieved simply through the use of off-the-shelf processors. In one embodiment, for damaged or otherwise inoperable signal processors located on a spacecraft, the remaining processors which are undamaged can be reconfigured through changing the machine language and binary to the field programmable gate arrays to change the core processor while at the same time maintaining undamaged components so that the signal processing functions can be restored utilizing a RAM-based FPGA as a signal processor. In one embodiment, multiple FPGAs are connected together by a data bus and are also provided with data pipes which interconnect selected FPGAs together to provide the necessary processing function. Flexibility in reconfiguration includes the utilizing of a timing and synchronization block as well as a common configuration block which when coupled to an interconnect block permits reconfiguration of a customizable application core, depending on the particular signal processing function desired. The result is that damaged or inoperable signal processing components can be repaired in space without having to physically attend to the hardware by transmitting to the spacecraft commands which reconfigure the particular FPGAs thus to alter their signal processing function. Also mission changes can be accomplished by reprogramming the FPGAs.